



The manufacturer may use the mark:



Revision 1.0 Feb 15, 2023  
Surveillance Audit Due  
Mar 1, 2026



# Certificate / Certificat

## Zertifikat / 合格証

Arm 2103-105 C022

exida hereby confirms that the:

### Arm Cortex-M55 Processor

Arm Ltd.

Cambridge, Great Britain

Has been assessed per the relevant requirements of:

**ISO 26262:2018 Parts 2, 4, 5, 7, 8 and 9**

**IEC 61508:2010 Parts 1 and 2**

and meets the requirements providing a level of integrity to:

**Systematic Capability: ASIL D / SIL 3 Capable**

#### Safety related function:

The Cortex-M55 Processor was developed as a HW Safety Element out of Context (SEooC) or compliant item, with the assumption that the following functions will be used in a safety related application context:

- Execution of instructions, generating the correct result and executing in the right order
- Correct response to stimuli like interrupts and events
- Correct usage of buses according to defined protocols
- Correct usage of coprocessors with a defined interface

#### Application restrictions:

The Cortex-M55 processor shall be used according to the requirements described in the Arm Cortex-M55 Processor Safety Manual.



*A. Grijp*  
Evaluating Assessor

*J. Koelhaas*  
Certifying Assessor

## Arm Cortex-M55 Processor

### Systematic Capability: ASIL D / SIL 3 Capable

#### Product Overview

The Arm® Cortex®-M55 Processor is a synthesizable soft-IP (i.e. RTL code) for integration into a safety related IC or system. It is a mid-range microcontroller class processor based on the Armv8.1-M architecture, featuring the M-class Vector Extension (MVE) to support compute applications such as Digital Signal Processing (DSP) and Machine Learning.

To support safety related applications, the Cortex-M55 includes several safety mechanisms to detect and control hardware faults (e.g. Dual-Core Lockstep, SECCED ECC for memories and caches, parity-based interface protection, etc.), or to prevent and control systematic failures on a system-on-chip and software level (e.g. Memory Protection Unit, Security Attribution Unit, exceptions, etc.).

#### Systematic Capability: ASIL D / SC 3 (SIL 3 Capable)

The Arm Cortex-M55 Processor has been developed as a Hardware Safety Elements out of Context (SEooC) or compliant item according to ISO 26262-10 and IEC 610508-2. The development, as documented by Arm, meets the applicable ASIL D design specification, implementation and verification requirements of ISO 26262, parts 4-9, as guided by ISO 26262-10, and the functional safety management requirements per ISO 26262-2. It also meets the applicable requirements for SIL 3 capability (SC 3) from IEC 61508, parts 1-2.

#### Hardware Safety Integrity (with Dual-Core Lockstep): ASIL D / SIL 3 (HFT=0)

The Arm Cortex-M55 Processor can be configured to include different safety mechanisms, to target different use cases and safety integrity levels.

*Note: Only configurations of Cortex-M55 Processor which include the Dual-Core Lockstep (DCLS) safety mechanism, are in scope of this certification.*

The FMEDA results show that the Cortex-M55, when used in a DCLS configuration, can fulfill the ASIL D requirements of ISO 26262-5, clause 8, including the ASIL D target values for the architectural metrics SPFM and LFM.

According to IEC 61508-2, the Cortex-M55 is a Type B element without hardware fault tolerance (HFT=0). When used in a DCLS configuration, the FMEDA results show that it can fulfill the SIL 3 requirements of IEC 61508-2, clause 7.4.4, including the SIL 3 target value for the SFF architectural metric.

It is the responsibility of the user and integrator of the Cortex-M55 processor, to adjust the FMEDA according to their actual IP configuration, and to re-evaluate the FMEDA results in the context of their safety related IC or system.

#### The following documents are a mandatory part of this certification:

Assessment Report: Arm 21/03-105 R021, V1 R0

Safety Manual: Arm Cortex-M55 Processor Safety Manual

FMEDA Report: Arm Cortex-M55 Processor FMEDA Report

Arm Cortex-M55  
Processor



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T-048, V4R2